Design and evaluate a 400 MSPS Software defined radio receiver

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***Abstract*— Software defined radio is a design of radio transceivers where components traditionally in the analogue domain are moved to the software domain proving increased flexibility and reusability. Achieving the ideal SDR receiver requires high speed and power efficient ADCs, in this work, time interleaving two 200MSPS 8bit ADCs and subsequent digital signal processing is discussed as a solution to receiving FM radio broadcasts. To evaluate the effectiveness of the design, measurement of signal to noise ratio, ADC mismatches and received signal integrity are discussed.**

***Index Terms*— Analog-to-digital converter (ADC)-based receiver, SDR**

I. Introduction

RADIO receivers are designed to receive and process electromagnetic signals, providing a basis for today's wireless communication devices. A generic radio receiver typically operates in a fixed frequency range with fixed signal encoding and is consequently commonly realised in an application-specific integrated circuit (ASIC) [1], which are optimized for performance and size without consideration to future development or changes.

To account for the growing proliferation of wireless communications devices, there has been increased use of the electromagnetic (EM) spectrum and increasing rate of change of encoding schemes and frequency reuse techniques. A modern cell phone is expected to adhere to multiple communication protocols [2] such as cellular voice and data (GSM, GPRS – 4G), personal area networks (WPAN) (Bluetooth), local area networks (WLAN) (Wi-Fi) and near-field communications (NFC) (Contactless payments) over a range spanning KHz – MHz. This list of protocols and bandwidth is expected to continue to increase with the adaption of next-generation standards (5G) enabling the connection of evermore devices.

One method of enabling this flexibility and functionality is software defined radio (SDR). SDR moves the generic radio receiver design from hardware to software, enabling changes to be made through software updates, even after system manufacture. Updates can enable new communication schemes/ frequencies to be used or if used in real-time, a single radio stage can be switched between protocols, reducing duplication, power consumption and circuit size.

The ideal SDR receiver design is an analogue to digital converter (ADC) connected directly to a broadband antenna so that all processing can be performed in software with the most flexible possible hardware. This operates under the principle that electromagnetic signals are received through the antenna and sampled by the ADC, before being digitally processed so that the encoded data is recovered. However, this design is not currently feasible due to the limited sample rate of ADCs and the cost of ADCs approaching these levels. Currently, this type of SDR receivers is limited to state-of-the-art space and military applications only [3].

The sample rate problem can be overcome by performing analogue processing before the signal is sampled; the signals are mixed to a fixed intermediate frequency which is lower than the received frequency and more coinvent to sample/process. However, this limits the bandwidth of the receiver due to sampling now only being performed on part of the received signal, reducing the flexibility of this design.

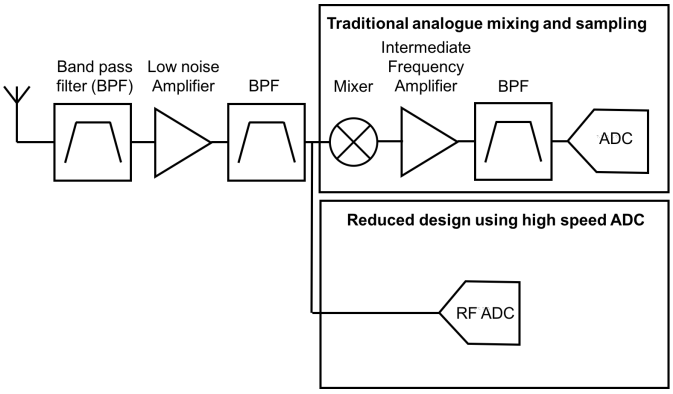

Figure 1 – Comparison of a generic radio receiver and direct sampling SDR architecture

An alternative to this method is discussed in this article, bringing radio receiver design closer to the ideal SDR model through direct RF sampling [4] of a wireless signal utilising multiple high-speed ADCs and time interleaving methods [5]. The design will then be evaluated with regards to signal to noise ratio, power consumption and price for an example received signal of an FM radio broadcast and 200MHz sine.

II. Economic, Legal, Social, Ethical and Environmental Context

In the United Kingdom, wireless transmissions are regulated by OFCOM, a UK government-approved regulatory and competition authority. Strict controls and penalties are in place for transmitting on frequencies without the appropriate license. Unintended transmissions could affect vital services such as GPS and emergency communications and as such, this project will be designed only as a receiver with no transmitting components. Where signals must be generated, for testing purposes the EM radiation from the cabling used will be considered and minimised.

Legal controls are also in place for receiving signals [6] for which you are not the intended recipient, considering this and the wide bandwidth of the SDR receiver, it is likely to capture signals not intended for public reception, therefore, data will be kept to a minimum and signal recovery will only be performed on signals intended to be received by the public.

III. Methodology

Figure 1 shows the overall receiver architecture of a direct RF sampling SDR. the system is sub-divided into the *Analogue front end, Sampling* and *Digital signal processing* sections. These subsections will be used as a guide to design a system performing within the project aims. The aims will then be assessed through measurements to decide if the specifications have been met.

A. Analogue front end

This design uses a DC-coupled non-inverting op-amp based amplifier design as a low-noise amplifier (LNA). The LNA amplifies the signal from the antenna so that it is at a level to utilise the maximum sample range of the ADC. DC Coupling was chosen to provide the ability to measure DC voltages that could appear on the analogue front end. The non-inverting design provides a lower input impedance as the input is directly into an op-amp pin, though is limited to gains of greater than 1, however, signals presented to the front end are very unlikely to be greater than the 1.5v ADC reference level.

Front-end suitability will be measured through the creation of a bode plot and then measurement of response at frequencies of interest.

B. Sampling

Sampling is performed by two identical 8-bit 200 MSPS ADCs. Discrete samples are taken from the continuous analogue input signal by the internal sample-and-hold contained within the ADC, the held value is then digitised through a pipelined process and output as an 8-bit parallel binary bus. This data is input to an Xilinx Artix-7 FPGA, through a buffer to prevent digital noise from the FPGA being coupled into the ADCs.

C. Digital signal processing

The high sample rate data from the ADCs are first mixed to bring the signals of interest to a baseband frequency enabling resampling to a lower sample rate. More efficient filtering can be performed on signals at lower sample rates as well as enabling data to be offloaded to a subsequent signal processing system such as MATLAB.

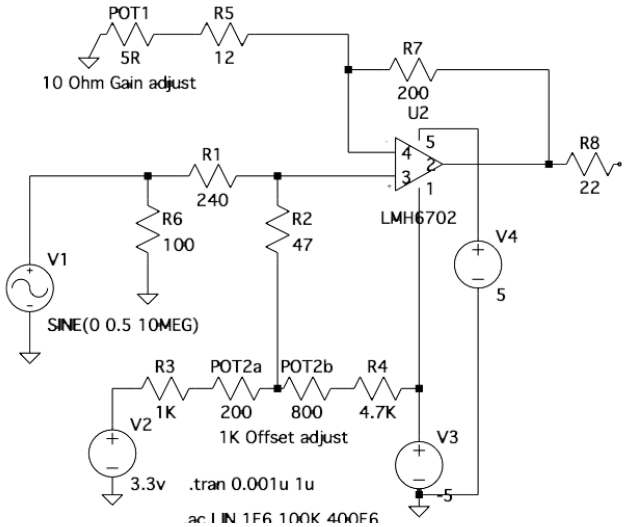

Figure 2 - Analogue front-end design

D. Measurement techniques

To assess the suitability of the design, signal to noise ratio (SNR) and power consumption measurements will be taken. SNR will be measured for an input 200MHz sine wave with amplitude close to the maximum range of the ADC to maximise the use of the ADCs dynamic range.

IV. Results and Evaluation

A frequency domain simulation of the analogue front end was performed using LTSPICE and is shown in Figure 3. From the simulation it can be seen that the circuit has a -3dB frequency of 370MHz, significantly above the maximum sampleable frequency of 200MHz. Over the range from DC – 200MHz there is an approximately constant gain of 1.1dB, providing some gain to the input signal. This gain is adjustable in circuit to and will be tuned for each input signal. Further measurements were not taken due to the lack of equipment with a frequency output of over 10MHz as if measurements had been performed, the gain would be constant over the DC – 10MHz range following the simulation results. This circuit is however indirectly tested through measurements taken while testing the digitization stage.

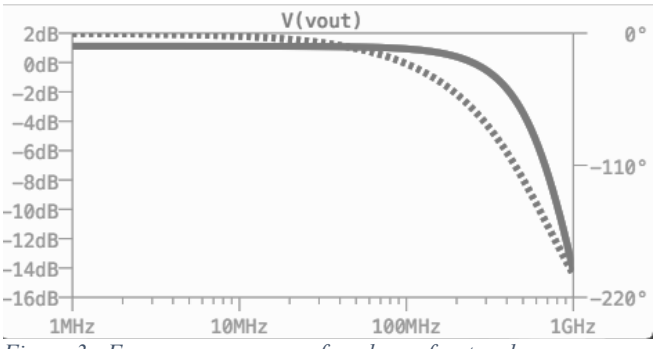

Figure 3 - Frequency response of analogue front end

The next measurements were performed on the digitisation stage, the ADCs were driven at the highest generatable clock frequency of 10MHz and input signals of varying frequencies were input. The digital output was then recorded using a logic analyser and subsequently processed. Figure 4, shows the digital output from a single ADC, measuring an input signal of 1 MHz at a sample rate of 10 MSPS. Although there is considerable noise, the frequency of the measured signal calculated from measuring five periods of the signal is correct at 1 MHz Showing the clocking of the ADCs is working as required as there are no time base inaccuracies. It can also be seen that there is no clipping of the signal as the high and low peaks do not extend beyond the graph axis, while also attempting to maximise the dynamic range of the ADC, as the signal uses approximately the full 0-256 range of the ADC.

While the speciation's stated the circuit would be tested using a 200MHz signal, in this case, it was not possible as the equipment provided could not reach these frequencies. It is expected that the circuit would operate largely the same due to the design being performed to meet a sample rate of 400 MSPS, enabling sampling of a 200MHz sine at the Nyquist rate.

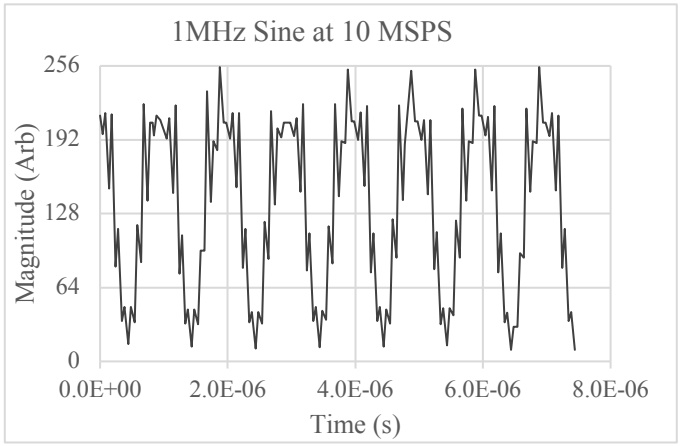

Figure 4 - 1 MHz signal sampled at 10 MSPS

To analyse the signal further, a discrete time Fourier transform has been performed (Figure 5). This shows the expected peak at 1MHz from the input signal, there are however other peaks at 2 MHz and 4 MHz. These frequencies are harmonics of the input signal and could possibly be caused by distortion in the test equipment generating the input signal. The specifications for the function generator states a -40dBc harmonic distortion which is a significantly smaller magnitude than that that measured in this case (-18dBc). Another possible cause of these peaks could be signals coupled from the 10MHz ADC clocks which due to aliasing and other under-sampling effects appear in the measured range [7].

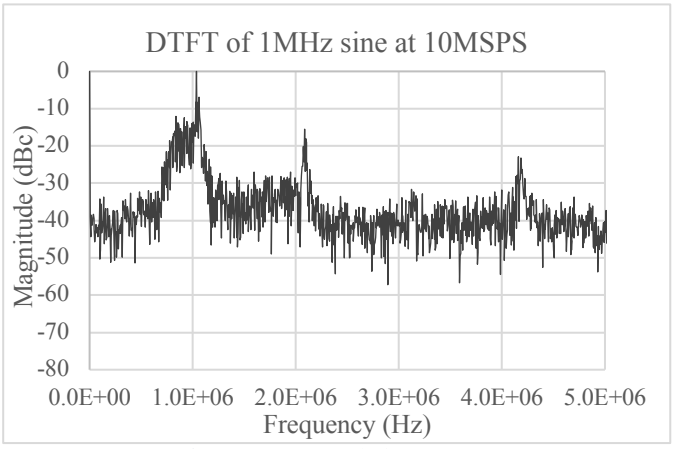

Figure 5 - DTFT of 1MHz sine sampled at 10MSPS

To minimise the effect of these peaks on the recovered signal, low pass filtering has been performed (Figure 6) and has subsequently reduced the peaks to a level less than the noise floor of the unfiltered signal. In this case, the noise floor of the unfiltered data is 41dB, this closely matches the 43.4dB value in the datasheet. This value also correlates with the ideal value 49.9dB from equation 1 which is the greatest possible value for an 8-bit ADC. This partially meets the specification for performing digital signal processing as it successfully removes spurious peaks from the recorded signal, it is however not been designed to demodulate any data and therefore fails to fully meet this requirement.

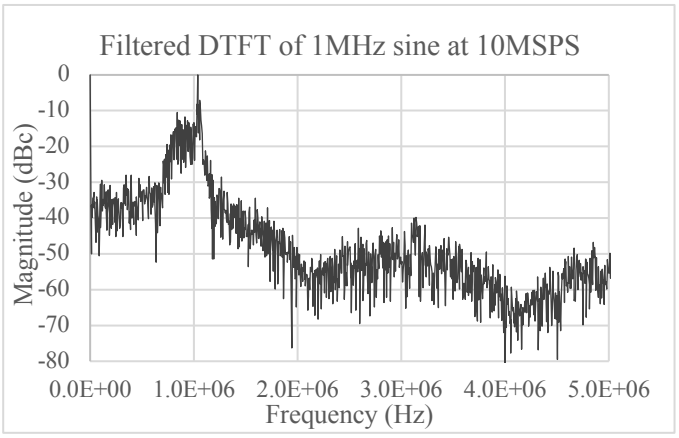

Figure 6 - Filtered DTFT of 1MHz Sine at 10MSPS

$$6.02N + 1.76 = 6.02 \cdot 8 + 1.76 = 49.9dB \quad (1)$$

Signal-to-noise ratio is a key design measure of the circuit allowing evaluation of noise introduced to a perfect input signal by the circuit. The measured SNR of the filtered data is 47.6dB (Figure 6). There was no specification requiring an SNR value, and hence it is sufficient to evaluate this design against similar designs. In comparison, a commercial FM receiver IC has an SNR of 48dB [8], however, this is an unfair assessment due to the FM reviver being tested at frequencies approaching 200MHz and amplitudes of 2.5mV compared to the 1Mhz and 50mV of the circuit under test. This greater amplitude provides conditions which are significantly easier to reduce noise.

Example data could not be found for a 1MHz receiver due to little use of this frequency for signal transmissions.

A key part of this design was to interleave the output of two ADCs however, again this was not possible due to lack of equipment. To test this, it is required to sync two signal generators reference frequencies, such that they would operate at identical frequencies and have the ability to generate a 180° phase shift between them. The Keysight 33210A does not have this capability as standard [9].

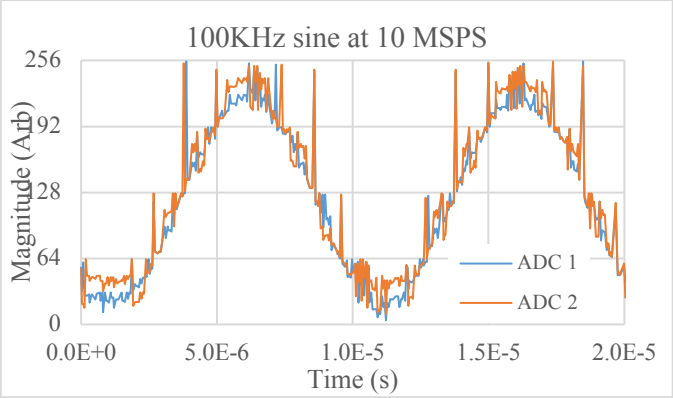

Figure 7 - Dual Channel sampled 100KHz sine

A measurement relevant to time interleaving that was still able to be performed around these limitations was the DC offset between channels [10]. It can be seen in 8 that there is a mean offset of 4.3 measurement steps between the two ADCs, as a percentage of the full-scale value, this is 1.66% or 24.6mV. It is expected that there would be a small constant difference between ADCs due to component tolerance in the voltage references which would be characterised and corrected in software. However, the measured difference exhibits noisy characteristics, significantly greater than the expected constant offset and would not be possible to compensate for in software, failing to meet the required specification for correction of mismatches between the ADCs. The value of 24.6mV was measured over a large period and assuming the noise is ideal would provide an accurate value for the constant offset between ADCs, allowing for partial achievement of this specification.

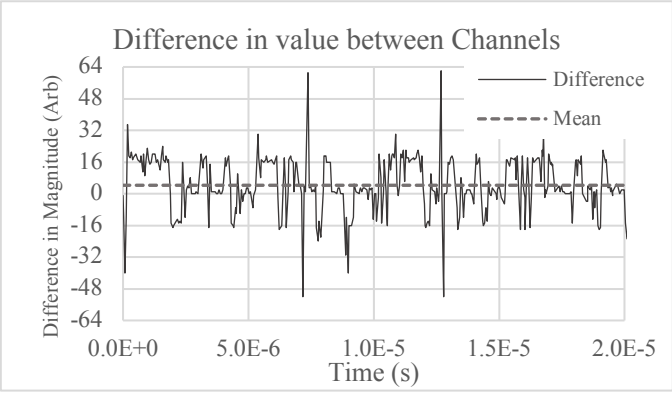

Figure 8 - Difference between the output of ADCs

V. Evaluation

The final aim of this work is to design a receiver suitable for receiving a broadcast FM radio station, and while progress has been made, there have been significant failures to meet specifications leaving the final design incapable of achieving this aim.

Some failed specifications can be attributed to lack of equipment, such as testing at a frequency of 200Mhz. Where this has occurred, there have been attempts made to negate the consequences by using the equipment that was available to produce measurements at lower frequencies providing data on the general operation of the design. It is expected that the characteristics exhibited at clock speeds of 10MHz will be significantly similar to those at 200MHz.

To fully characterise the design, it is required for every specification be achieved as each is a part of a system processes the data so that it is suitable for the next part of the system to further process. If one part is un-operational the data cannot travel to the subsequent parts. Overcoming this problem was achieved by using test and measurement equipment to provide substitute signals allowing for each sub-system to be tested individually. While testing the ADCs for example, multiple function generators were used in place of the antennas and FPGA clock generators, while oscilloscopes and logic analysers replaced the FPGA signal processing providing the measurements used in the previous section.

The first further work required would be to continue the design such that it meets the aims of the project. Once completed and before the addition of features, the design should be improved in regards of its SNR, this could be achieved through the use of more stable voltage references, for example, designs independent of voltage supply fluctuations. Additional work could be performed in improving the reconfigurability of the design, for example, an interface to change the FPGA DSP design without complete reprogramming. The additional flexibility would open the opportunity to use the hardware with powerful SDR software such as SDR# increasing the usability of the circuit through graphical user interfaces.

VI. Conclusions

Significant progress has been made in developing the hardware design of an SDR receiver that provides a flexible base for sampling applications up to 400MSPS. Characterised by a bandwidth of 370MHz, 8-bit resolution and a 47.6dB SNR.

Moderate progress has been made towards developing a digital signal processing solution capable of using the hardware to receive an FM radio signal, with the current design capable of removing spurious peaks from a 1MHz signal sampled at 10MHz. While designing, system flexibility has been maximised to allow for the widest possible application of this design.

VII. Refrences

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