RF Direction of Arrival Estimation Using a Linear Antenna Array

Lawrence Carslake, Oliver Johnson, Edward Pipe & Wei Sam

Introduction

What is DOA?

- Direction of Arrival Estimation.
- Find direction that a source is coming from.
- Can be done with antenna array.

Why is it useful?

- Cheap, Fast, Reliable.
- Can be miniaturised.

What does this mean?

- Miniaturisation for mobile telecoms.
- 4G / 5G MIMO systems

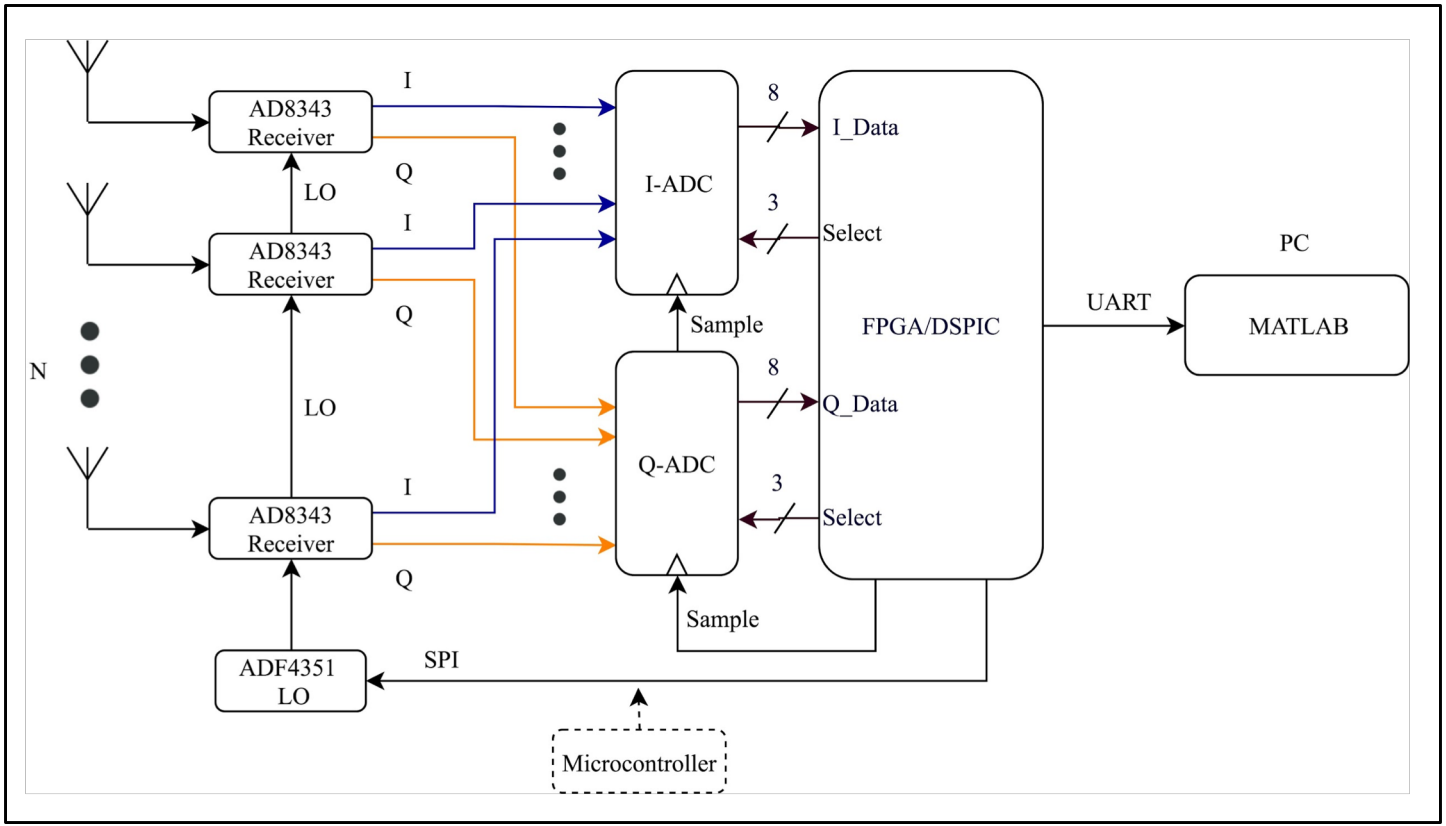
How can we do it?

- Build receiver and antenna array.
- Read data using FPGA
- Perform DSP

Project Aims and Objectives

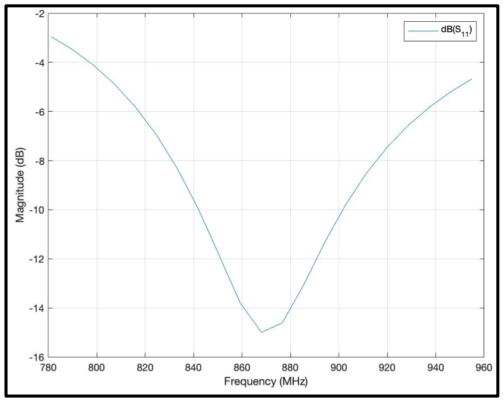
- To design, build and test a demo RF DOA system, which includes:
  - Design and test bespoke antennas to be implemented into (phased) array
  - Design, build and test Quadrature receiver with operational frequency range 50MHz - 1GHz
  - Design and simulate DOA algorithms in Matlab
  - Design and implementation of ADC hardware and supporting FPGA digital architecture
  - Implementation of DSP on FPGA
  - Design of GUI for data presentation
  - Whole system integration
- Stretch Goals: Apply to GSM Bands.

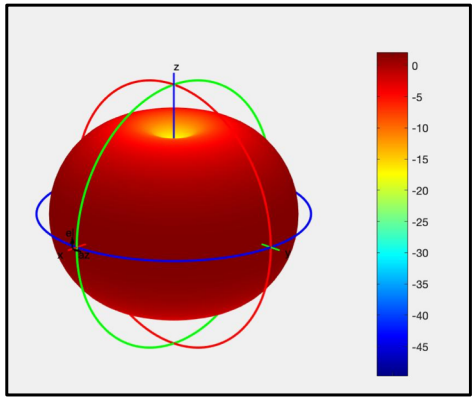
System Overview – Ed

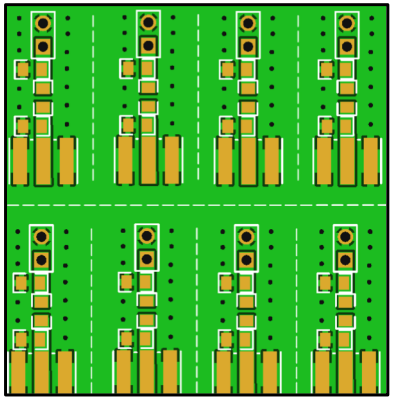


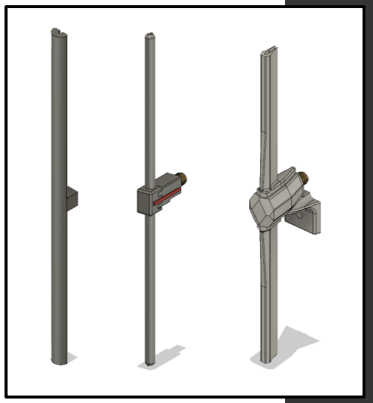
Antenna Design – Oli

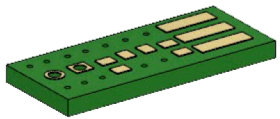
- Commercial 868MHz Antenna ~ £5. Aim is to produce cheap alternative.
- Monopole design simulated, constructed and tested. S11 at -6dB (Tested)
- Dipole design simulated, constructed and tested. S11 at -15dB (Tested)
- Maximum power transfer to receiver to be achieved using matching networks.
- To make rigid, reproducible design, all integrated onto a PCB design. Cased for protection.
- Needs constructing and matching network values need to be designed.





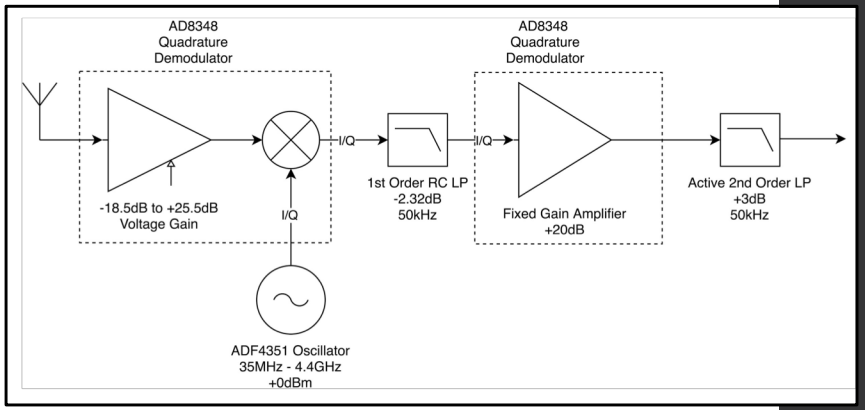






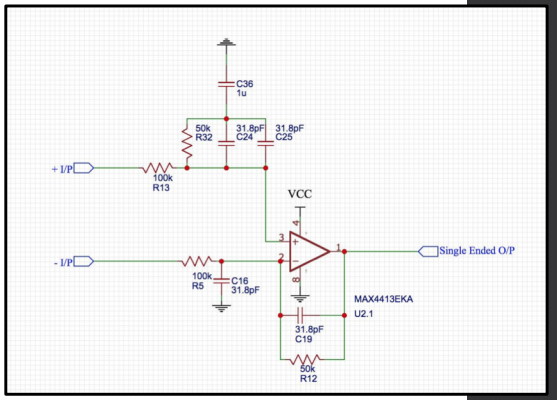
Receiver System – Ed

- Aims
  - Build a receiver to mix a test tone from RF to baseband
  - Perform Signal conditioning to prepare the baseband tone for DSP.



- Progress
  - Prototype Receiver circuit constructed and tested with local oscillator.
- Work To Be Carried Out
  - Design review of current system
  - Final circuit and layout design, including local oscillator distribution.

Filter Design – Ed



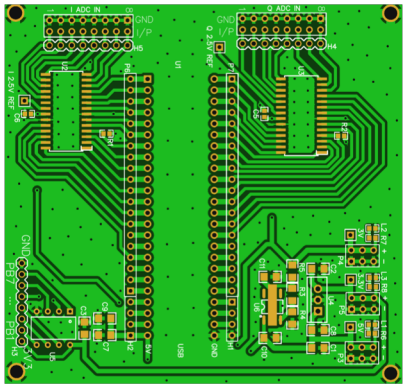
- Aims
  - 50kHz LP Baseband filter to prevent overdriving of the fixed gain amplifier
  - 50kHz LP Anti-Aliasing filter before the ADC.

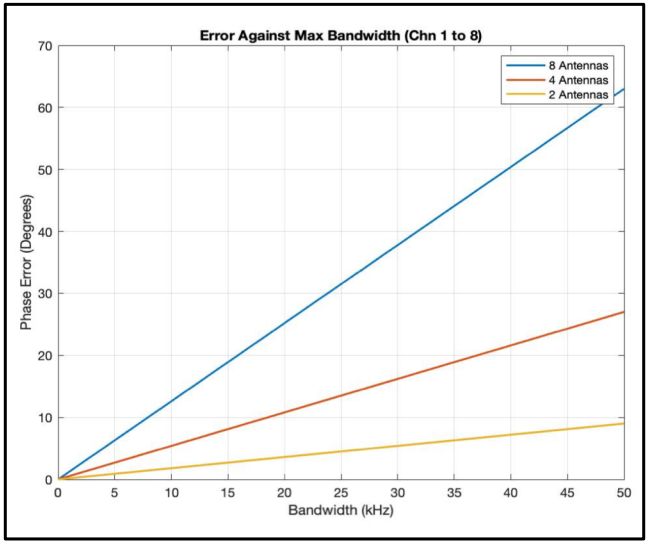
- Progress
  - Baseband filter currently 1st order RC network due to layout constraints. Initial 5th order LC design was difficult to fit around pins on chip.
  - 2nd order active filter for anti-aliasing. Used non-standard design technique* to minimise component usage.
  - Both simulated in LTSpice.
  - Constructed, characterised and verified.
- Work to be carried out
  - In system verification

* D. KNOLLMAN, “Designing with op amps: Single-formula technique keeps it simple,” Lucent Technologies, 02/03/1998.

ADC System – Oli

- Aims
  - Convert analogue baseband signal to digital for DSP
  - Requires maximum RF capture bandwidth
- Progress
  - 8-bit ADCs chosen (2 MSPS - 250 kSPS per channel)
  - Current maximum BW evaluated
  - ADC/FPGA board PCB designed, built and tested
- Work to be carried out
  - New ADC or sample and hold system to increase maximum BW





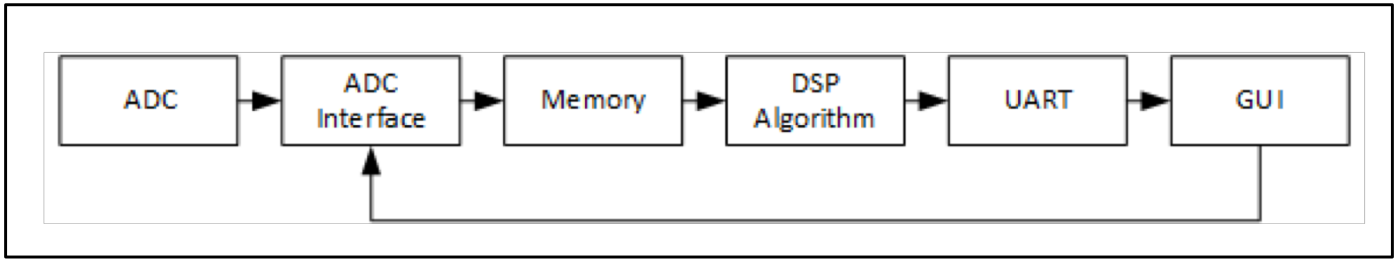
Oscillator Design – Lawrence

- Aims
  - SPI control of ADF4351 Local Oscillator development board.
  - Integration of ADF4351 development board into RF PCB.
  - Work with the RF receiver team to ensure suitability.
- Progress
  - Controllable from a GUI over the range of 35 MHz - 4.2GHz
  - Based on open source control libraries for ADF4351, serial, and SPI
  - Loop filter characterisation for reduction of spurious peaks
- Work to be carried out
  - Development of a PCB to professionalise
  - Design RF Power splitter for LO distribution
  - Integrate GUI with DSP GUI

FPGA Design – Lawrence

- Aim is to Implement a DOA algorithm onto system hardware
- FPGA enables higher speed sampling but at a higher cost

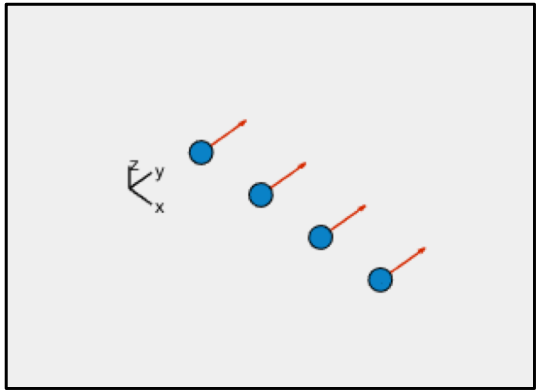
ADC Interface: Tested and finished
Memory: Started, designed and waiting to be implemented
DSP: Planned
UART: Initial research into design
GUI: First phase complete

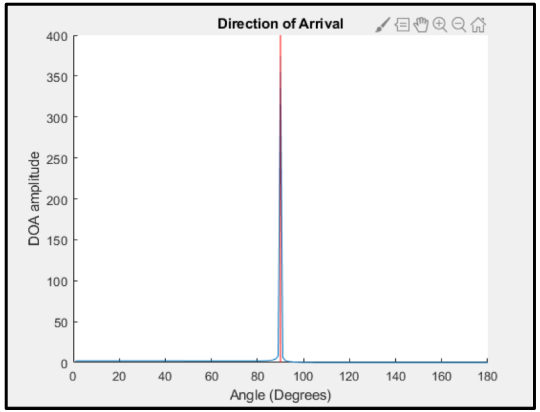


DOA Estimation Algorithm – Wei

- Tested with 4 element Uniform Linear Array (ULA)
  - Linear array geometry allows for a response matrix to be calculated.

- Single source with fixed angle simulated in MATLAB/Simulink.
- Received signal from array input – take covariance matrix and decompose.
- MUSIC derivative algorithm – Look for peaks in the spatial spectrum





DOA Estimation Algorithm – Wei

Aims

- Research and develop a suitable DOA estimation algorithm that can be implemented on an FPGA.

Progress

- Simulated signals in Simulink – currently set up for a ULA of 4 isotropic antennas.
- Testing of algorithm in MATLAB – Currently working for certain angles, but difficulties at others.

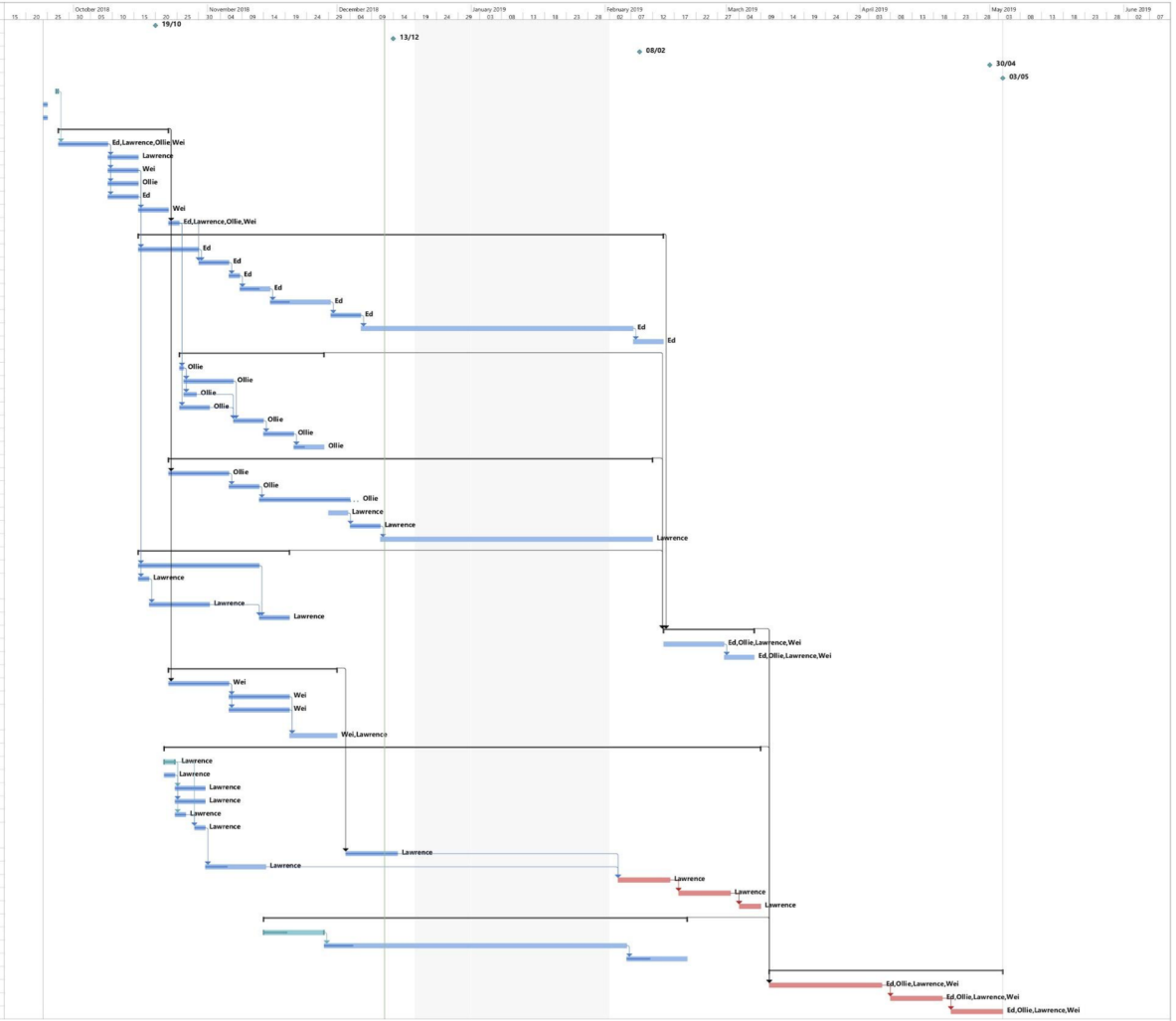
Work to be carried out

- Review algorithm, determine SNR of algorithm
- Implementation of algorithm onto FPGA via Xilinx System Generator or Model Composer

Project Management – Where we are now

Antennas	Final Construction and Testing
Receiver	Testing - 15/02/19
Oscillator	Complete
ADC	Complete
ADC interface	Complete
Memory	Designed - 15/02/19
DSP	In Simulation - 15/02/19
GUI	Building - 19/02/19

ID	Task Name	Finish	% Complete
1	Initialisation report deadline	Fri 19/10/18	100%
2	Interim Presentation deadline	Thu 13/12/18	0%
3	Interim Report deadline	Fri 08/02/19	0%
4	Final Presentation deadline	Tue 30/04/19	0%
5	Final report deadline	Fri 03/05/19	0%
6	Initialisation meeting	Thu 27/09/18	100%
7	Initialisation Report	Mon 24/09/18	100%
8	Interim presentation prepration	Mon 24/09/18	100%
9	**Research**	**Mon 22/10/18**	100%
10	General Background	Mon 08/10/18	100%
11	ADC Research	Mon 15/10/18	100%
12	DOA Algorithms Research	Mon 15/10/18	100%
13	Antenna Research	Mon 15/10/18	100%
14	Reciever Research	Mon 15/10/18	100%
15	DSP Research	Mon 22/10/18	100%
16	**Finalise Project Aims and Objectives**	Thu 25/10/18	100%
17	**Receiver**	**Thu 14/02/19**	**52%**
18	Design PCB 1st draft	Mon 29/10/18	100%
19	Order PCB components	Mon 05/11/18	100%
20	Build PCB	Thu 08/11/18	100%
21	Test receiver by itself	Thu 15/11/18	50%
22	Design PCB 2nd draft	Thu 29/11/18	25%
23	Order PCB Components	Thu 06/12/18	100%
24	Build receiver PCB	Thu 07/02/19	0%
25	Verify PCB and design	Thu 14/02/19	0%
26	**Antenna**	**Tue 27/11/18**	**92%**
27	Design Wire antenna	Fri 26/10/18	100%
28	Simulate antenna design	Tue 06/11/18	100%
29	Construct Wire antenna	Mon 29/10/18	100%
30	Order alternative Antenna	Thu 01/11/18	100%
31	Test Antennas with VNA	Tue 13/11/18	100%
32	Compare Built Antenna with Bought	Tue 20/11/18	100%
33	Order/Construct final number of ante	Tue 27/11/18	50%
34	**ADC**	**Mon 11/02/19**	**74%**
35	Schematic	Mon 05/11/18	100%
36	PCB Design draft 1	Mon 12/11/18	100%
37	Order	Wed 05/12/18	100%
38	Construct	Mon 03/12/18	0%
39	Test	Mon 10/12/18	100%
40	Re-evaluate	Mon 11/02/19	0%
41	**Oscillator**	**Mon 19/11/18**	100%
42	Order module	Mon 12/11/18	100%
43	Decide interfacing between micro controller and FPGA	Thu 18/10/18	100%
44	Code Control	Thu 01/11/18	100%
45	Oscillator Control Testing	Mon 19/11/18	100%
46	**Analogue Front End Integration**	**Thu 07/03/19**	**0%**
47	Test	Thu 28/02/19	0%
48	Re-evaluate	Thu 07/03/19	0%
49	**DSP**	**Fri 30/11/18**	**77%**
50	Start Testing Algorithms	Mon 05/11/18	100%
51	Synthesize I/Q for 2 receivers	Mon 19/11/18	100%
52	Simulate Beamforming with two dummy I/Q signals	Mon 19/11/18	100%
53	Hardware requirement decision	Fri 30/11/18	0%
54	**Digital Hardware**	**Fri 08/03/19**	**51%**
55	Design Pin in/out and transceivers	Wed 24/10/18	100%
56	Calculate core clock speed	Wed 24/10/18	100%
57	Merge interface with IO	Wed 31/10/18	100%
58	Check Clocking	Wed 31/10/18	100%
59	Define hierarchies	Fri 26/10/18	100%
60	Generate IP and re-evalulate device	Wed 31/10/18	100%
61	Implement algorthm in system design	Fri 14/12/18	100%
62	Build RTL submodules	Wed 14/11/18	33%
63	Assemble and validate	Fri 15/02/19	0%
64	Final Validation	Fri 01/03/19	0%
65	Code upload and testing	Fri 08/03/19	0%
66	**GUI**	**Tue 19/02/19**	**33%**
67	Design	Tue 27/11/18	33%
68	Build	Tue 05/02/19	33%
69	Validate	Tue 19/02/19	33%
70	**System Integration**	Fri 03/05/19	0%
71	Combine modules	Fri 05/04/19	0%
72	Test Beamforming for 2 antennas	Fri 19/04/19	0%
73	Test for all Antennas	Fri 03/05/19	0%



Thank you for Listening.

Any Questions?